PROJECT IDEAS · ECE / ENTC

Final year projects for *ECE*

The best final year projects for ECE are ones you can **build, measure and demo**: a design, a board or a radio link that does one job, plus a number that proves it works.

Last updated 2026-10-10

That number might be a timing report, a BER curve against theory or a measured S11. Below are 27 ideas across VLSI, embedded systems, communication and SDR, DSP, RF and antenna, robotics and control, and edge vision. Each names the board or tool, what you measure, a viva angle and a rough cost band. EnTC and EXTC students can use the same list.

KEY POINTS

- **27 ideas in seven domains:** VLSI, embedded systems, communication and SDR, DSP, RF and antenna, robotics and control, and edge vision.
- **A strong ECE project has three parts:** something you build, something you measure against a reference, and a demo that works in the room.
- **VLSI needs no paid tools.** From the 2026.1 release, AMD's Vivado has a free BASIC tier covering 7-series parts such as Artix-7; Icarus Verilog, Verilator and GTKWave are open source.
- **EnTC and EXTC students can use the same list.** Both are Maharashtra names for Electronics and Telecommunication Engineering, which covers the same core as ECE.
- **Simulation-only ideas need no hardware,** and most board-based ideas need roughly ₹5,000 or less of parts.

What makes a good final year project for ECE?

Examiners want to see a circuit, a chip or a signal behave the way your theory says it should. A strong project has three parts:

- **Something you build:** an RTL design, firmware, a PCB, a GNU Radio flowgraph or a robot.
- **Something you measure against a reference:** a timing report, a BER curve over the theoretical one, measured S11 against simulation, or a step response against the model.
- **A demo that works in the room:** a board that runs, a radio that receives, or a plot you can regenerate live.

Level: Beginner is one tool and one measurement; Intermediate adds a comparison or real-time limits; Advanced means a larger design or field testing. **Cost bands** follow our IoT ideas page: **Low** is roughly ₹2,000 or less of parts, **Medium** about ₹2,000–5,000, **High** above ₹5,000. **Free** means software only; **lab** means equipment you borrow from the department. Rough bands, not quotes.

> **Topic ideas, not delivered projects**
> Every row below is an idea to discuss with your guide. Our 8 delivered case studies are M.Tech and M.E. projects in computer science and AI, not ECE builds, so no result on this page comes from our own ECE work.

Which VLSI projects can you build on an FPGA with free tools?

Write the design in Verilog or VHDL, prove it with a testbench, then run it on your lab's FPGA board. Synthesis and timing reports give you numbers to compare before any hardware.

VLSI and FPGA project ideas

IDEA	BOARD OR TOOL	WHAT YOU MEASURE	VIVA ANGLE	COST BAND
IDEA · BEGINNER **UART, SPI and I2C controllers with a self-checking testbench**	Verilog or VHDL; Icarus Verilog and GTKWave or Vivado's simulator; the lab FPGA board	Error-free transfers at each baud rate, LUTs, flip-flops and maximum clock	Self-checking testbenches, and how a two-flop synchroniser handles an asynchronous input	Free in simulation; lab board
IDEA · INTERMEDIATE **Array, Booth and Wallace-tree multipliers compared**	Verilog; Vivado or Quartus Prime Lite synthesis with DSP blocks switched off	LUTs, critical-path delay and estimated power for 8-, 16- and 32-bit versions	Why the fastest multiplier is rarely the smallest	Free
IDEA · INTERMEDIATE **Fixed-point FIR filter on an FPGA**	Coefficients from MATLAB or SciPy; Verilog or VHDL checked against the software model	SNR against the floating-point filter per word length, resources, throughput	How word length sets quantisation noise	Free in simulation; lab board
IDEA · ADVANCED **A small RISC-V (RV32I) processor core**	Verilog; test programs from the RISC-V GNU toolchain, checked against the Spike simulator	Cycles per instruction and maximum clock, single-cycle against five-stage pipeline	Forwarding against stalls, and why branches hurt a pipeline	Free in simulation; lab board
IDEA · ADVANCED **RTL to layout with open-source ASIC tools**	LibreLane, the successor to OpenLane, with the open SkyWater SKY130 process design kit	Area, timing slack and power after layout, beside the FPGA numbers	LUTs against standard cells; what DRC and LVS catch	Free

Free tools, and their limits. From the 2026.1 release, AMD's Vivado has a free BASIC tier, renewed yearly, covering 7-series parts such as Artix-7 and Spartan-7; its simulator is capped at 50,000 design instances. Altera's Quartus Prime Lite is free for its MAX, Cyclone IV, Cyclone V and Cyclone 10 LP devices, and the bundled Questa Starter simulator needs a free licence. Icarus Verilog, Verilator and GTKWave are open source. Checked on 2026-09-29.

What are good embedded systems projects for ECE?

An embedded project earns its marks on timing and power, not on how many sensors it has. Measure what the firmware actually does.

Embedded systems project ideas

IDEA	BOARD OR TOOL	WHAT YOU MEASURE	VIVA ANGLE	COST BAND
IDEA · INTERMEDIATE **Multi-sensor logger on FreeRTOS**	STM32 Nucleo (Arm Cortex-M), FreeRTOS, microSD card	Task jitter on a logic analyser, CPU load, samples dropped under stress	Priority inversion and priority inheritance	Low to Medium
IDEA · INTERMEDIATE **Two-node CAN bus, like a car's ECUs**	Two STM32 boards, SN65HVD230 transceivers, 120 Ω termination	Latency, bus load, error counters when a node drops	How arbitration by message ID avoids collisions	Medium
IDEA · INTERMEDIATE **Battery life of a sensor node, measured**	STM32L4 Nucleo sleep and stop modes, an INA219 current sensor	Current per mode and estimated battery life, checked by a real run	Why sleep current usually decides battery life	Low to Medium
IDEA · ADVANCED **Fail-safe firmware update with your own bootloader**	STM32, two firmware slots, CRC-32 check, updates over UART	Update time; recovery after power is cut mid-update	Why you verify an image before jumping to it	Low

Keyword spotting and other TinyML builds sit on the IoT ideas page, so they are not repeated here.

Which communication and SDR projects work for a final year?

Communication projects are strongest when a simulated curve meets a measured one: start in MATLAB or Python, then take one link into the air.

Communication and software-defined radio project ideas

IDEA	BOARD OR TOOL	WHAT YOU MEASURE	VIVA ANGLE	COST BAND
IDEA · BEGINNER **BER curves for BPSK, QPSK and 16-QAM**	MATLAB or Python; AWGN and Rayleigh channels	Simulated BER against Eb/N0, over the theoretical curves	Why 16-QAM needs more power for the same BER	Free
IDEA · INTERMEDIATE **FM and aircraft (ADS-B) receiver in GNU Radio**	An RTL-SDR Blog V4 dongle (receive-only, 500 kHz to 1.766 GHz) with GNU Radio	FM station SNR; ADS-B messages decoded per hour at 1090 MHz for two antennas	Sampling and decimation	Medium
IDEA · INTERMEDIATE **LoRa link budget checked in the field**	Two ESP32 boards with SX1276 modules for India's 865–867 MHz band	RSSI, SNR and packet delivery against distance, beside a path-loss model	How spreading factor trades data rate for range	Low to Medium
IDEA · ADVANCED **OFDM link with channel estimation, simulated**	MATLAB or Python; least-squares and MMSE estimators, multipath channel	BER against SNR per estimator and cyclic-prefix length	What the cyclic prefix does to a multipath channel	Free

RTL-SDR range from the RTL-SDR Blog V4 release notes; India's LoRaWAN plan from The Things Network.

The SDR idea only receives public broadcasts. If your project transmits, use a cable with attenuators or a licence-exempt band within its power limit, and clear it with your lab in-charge. The LoRa pair can also carry a sensor from the LoRa farm network idea.

Which DSP projects can you do in MATLAB or Python?

DSP needs no hardware to start. The work is in the comparison: two methods, one signal, the same metric.

Digital signal processing project ideas

IDEA	BOARD OR TOOL	WHAT YOU MEASURE	VIVA ANGLE	COST BAND
IDEA · BEGINNER **FIR and IIR filters designed to one specification**	MATLAB Signal Processing Toolbox or scipy.signal	Order, ripple and group delay for windowed FIR, Parks-McClellan, Butterworth and elliptic designs	When linear phase matters	Free
IDEA · INTERMEDIATE **ECG denoising and QRS detection**	MATLAB or Python, with the open MIT-BIH Arrhythmia and Noise Stress Test databases on PhysioNet	SNR gain at known noise levels; QRS sensitivity against the beat annotations	Why electrode-motion noise can look like a heartbeat	Free
IDEA · INTERMEDIATE **Real-time audio equaliser on a microcontroller**	STM32 (Cortex-M4F), CMSIS-DSP biquads, an I2S codec	Latency, CPU load per stage, response from a sine sweep	Fixed point against floating point	Low to Medium
IDEA · INTERMEDIATE **Speech enhancement: spectral subtraction against Wiener filtering**	Python or MATLAB; your recordings plus noise at known SNRs	Segmental SNR gain and a blind listening test	Where 'musical noise' comes from	Free

Picked an ECE idea?

Send it with your branch, your lab's boards and your review dates. The consultation is free.

Message before 7 pm for a reply today.

Free consultation →

WhatsApp

What RF and antenna projects can you simulate and measure?

Simulate first, then fabricate and measure. Free tools are enough; use licensed suites such as Ansys HFSS, CST Studio Suite or Keysight ADS only if your lab already

has them.

RF and antenna project ideas

IDEA	BOARD OR TOOL	WHAT YOU MEASURE	VIVA ANGLE	COST BAND
IDEA · INTERMEDIATE **2.4 GHz microstrip patch antenna**	Design equations, then openEMS (free) or your lab's HFSS or CST; FR-4 PCB	S11 and bandwidth, simulated against measured on a VNA that reaches 2.4 GHz (a LiteVNA-64 does; a NanoVNA-H4, rated to 1.5 GHz, does not)	Why FR-4 tolerances shift the resonance	PCB Low; lab VNA (High if bought)
IDEA · INTERMEDIATE **Microstrip low-pass filter**	Qucs-S (free), openEMS check, FR-4 PCB	Cutoff and insertion loss, designed against measured	How line sections stand in for L and C	PCB Low; lab VNA
IDEA · ADVANCED **Phased-array beam steering, simulated**	Array-factor model in Python or MATLAB	Beam direction, beamwidth and side lobes against spacing and phase step	Why spacing over half a wavelength creates grating lobes	Free

Which robotics and control projects suit ECE students?

Control projects give you the cleanest viva: a model, a controller and a logged response you can compare with it.

Robotics and control project ideas

IDEA	BOARD OR TOOL	WHAT YOU MEASURE	VIVA ANGLE	COST BAND
IDEA · BEGINNER **DC motor speed control: on-off against PID**	Arduino or ESP32, encoder motor, motor driver	Rise time, overshoot and steady-state error	Each PID term, and integrator wind-up	Low
IDEA · BEGINNER **PID line follower**	Arduino, IR sensor array, two-motor chassis	Lap time and line error at different gains	Why the derivative term stops the weaving	Low

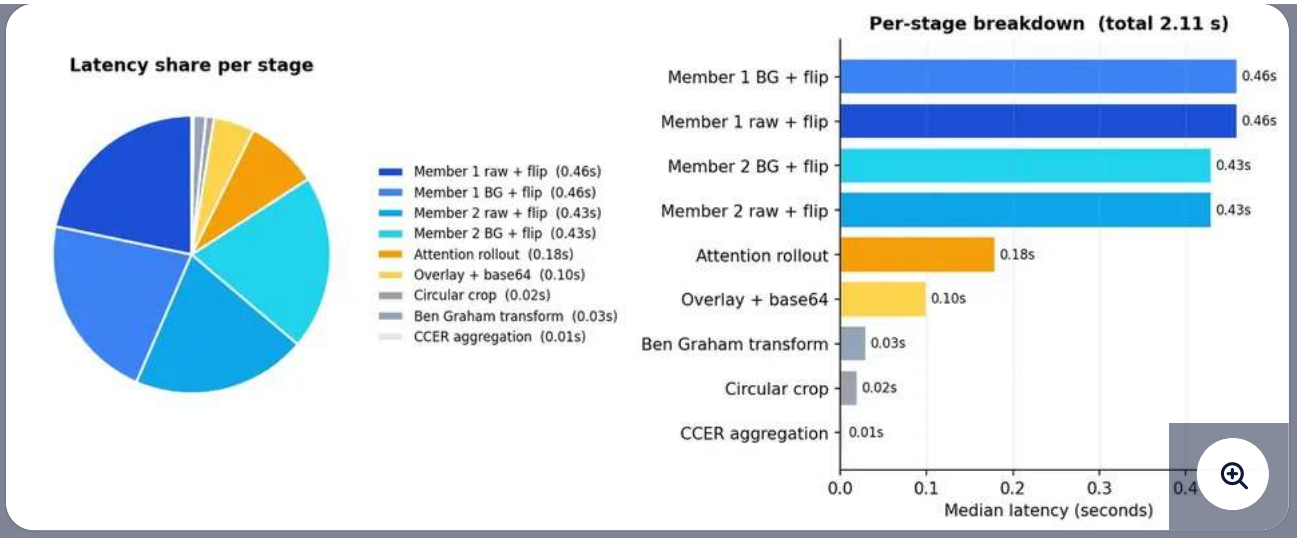
IDEA	BOARD OR TOOL	WHAT YOU MEASURE	VIVA ANGLE	COST BAND
IDEA · INTERMEDIATE **Self-balancing two-wheel robot**	ESP32, MPU6050 IMU, encoder motors	Tilt spread and recovery after a push; PID against LQR	Complementary against Kalman filter for tilt	Medium
IDEA · ADVANCED **Mapping robot with ROS 2 and a 2D LiDAR**	Raspberry Pi 5, RPLIDAR A1, ROS 2 with slam_toolbox	Map error against measured room sizes; drift over a loop	How loop closure corrects drift	High

What edge vision projects can run on a small board?

Edge vision is where ECE meets AI: the frame rate, memory and power budget matter as much as the model.

Edge vision project ideas

IDEA	BOARD OR TOOL	WHAT YOU MEASURE	VIVA ANGLE	COST BAND
IDEA · INTERMEDIATE **Driver drowsiness alert**	Raspberry Pi 5 and camera, MediaPipe Face Landmarker	Alert delay, and false alarms per hour by day and night	Why frames stay on the device	High
IDEA · ADVANCED **Doorway people counter on a microcontroller**	ESP-EYE (ESP32) with an 8-bit Edge Impulse FOMO model	Count error, time per frame, current draw	Accuracy lost to 8-bit quantisation	Medium
IDEA · INTERMEDIATE **Sign-language alphabet recogniser**	Webcam or Pi 5, MediaPipe Hand Landmarker, a classifier on 21 landmarks	Per-letter accuracy on unseen signers, frames per second	Why landmarks beat raw pixels	Free on a laptop; High on a Pi



Latency breakdown Per-stage latency from a delivered M.Tech project (a CS/AI web app for retinopathy grading, not an ECE build). Time your edge-vision pipeline stage by stage in the same way.

Where do IoT projects fit for ECE students?

IoT has its own list: 33 IoT project ideas, each with the board, sensors, a dashboard, a cost band and safety rules for mains-powered builds, so they are not repeated here. To give an IoT build a stronger ECE angle, add one measurement from this page: a LoRa link budget, a measured battery life or a filtered sensor signal.

Are ECE, EnTC and EXTC the same branch?

For choosing a project, yes. In Maharashtra the branch is usually called Electronics and Telecommunication Engineering. Colleges under the University of Mumbai shorten it to **EXTC**, and colleges under Savitribai Phule Pune University (SPPU) write **E&TC** or **EnTC**. Most other universities call it Electronics and Communication Engineering, or **ECE**.

The core subjects are much the same: signals and systems, circuits, communication, electromagnetics, VLSI and embedded systems. SPPU's E&TC

syllabus (2019 course), for example, has VLSI Design and Technology and Radiation and Microwave Theory in the final year. So every idea here fits an EnTC or EXTC final year project; only the report template and review schedule differ, and those come from your department.

How do you turn an idea into an IEEE project for ECE?

An IEEE project for ECE starts from a recent paper in an IEEE journal or conference, such as *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, the *IEEE Sensors Journal* or *IEEE Access*. You reproduce its main result, then add one change you can measure.

Want to start from a published paper? Our IEEE base papers for ECE projects has 24 open-access papers from 2023 to 2026, each checked against its DOI, with what to reproduce for B.Tech and what to change for M.Tech.

1. **Choose a paper you can reproduce.** Check its dataset, board or tool first; see how to select a base paper.
2. **Match the baseline first**, with the paper's own method on your setup.
3. **Change one thing**, such as a faster adder or a better estimator, and measure the gain on the same test.
4. **Write it up** using our IEEE paper format guide.

Lists of "latest IEEE projects for ECE 2026" are usually bare paper titles. Search IEEE Xplore for your domain, filter to recent years, and keep papers you can build or simulate. If your guide wants a published base paper, see our IEEE projects page for how that work runs. In M.Tech or M.E.? See M.Tech projects in VLSI, embedded systems and signal processing.

Frequently asked questions

What is the best final year project for ECE?

The one you can build, measure and demo within your time and budget: one board or tool and one clear measurement, such as a BER curve against theory or an FPGA timing report. Pick the domain you enjoyed most, because examiners will ask why you chose it.

Can I do a VLSI project without paid tools?

Yes. From the 2026.1 release, AMD's Vivado has a free BASIC tier covering 7-series FPGAs such as Artix-7, with a capped simulator. Quartus Prime Lite is free for Altera's MAX, Cyclone IV, Cyclone V and Cyclone 10 LP devices. Icarus Verilog, Verilator and GTKWave are open source, and LibreLane with the SKY130 kit takes RTL to layout at no cost.

Is EnTC the same as ECE for final year projects?

For choosing a project, yes. EnTC (or E&TC) and EXTC are Maharashtra names for Electronics and Telecommunication Engineering, which covers the same core as ECE. Only the report format and review schedule differ, and those come from your department.

What are good IEEE projects for ECE in 2026?

Start from a paper published in the last two or three years in your domain, reproduce its main result, then change one thing and measure the gain. The VLSI, embedded, communication and DSP ideas on this page can each be anchored to an IEEE base paper in that way.

How much does an ECE final year project cost?

Simulation-only ideas, such as VLSI synthesis, BER curves and DSP, need no hardware. Most board-based ideas here are Low or Medium, roughly ₹5,000 or less of parts; a Raspberry Pi 5, a LiDAR or a VNA costs more. Rough bands, not quotes: ask what your lab already has.

Can The Ultimate Project World help with an ECE project?

Yes. ECE and EEE are among the branches we support. Share your idea, the boards your lab has and your review dates in the free consultation, and we will tell you exactly which parts we can take on, such as the code, the report, the PPT and viva preparation.

RELATED SERVICES

From idea to a project you can present

IEEE projects
Start from a published base paper and extend it. →

Final-year projects
How the build, report, PPT and viva prep work. →

Report & PPT
Black book chapters and review slides. →